



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,491	07/24/2003	James E. Jaussi	10559-554002 / P12574C	2001
20985	7590	06/08/2005	EXAMINER	
FISH & RICHARDSON, PC			ENGLUND, TERRY LEE	
12390 EL CAMINO REAL			ART UNIT	
SAN DIEGO, CA 92130-2081			PAPER NUMBER	

2816

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

*Supplemental*  
**Notice of Allowability**

Application No.

10/626,491

Examiner

Terry L. Englund

Applicant(s)

JAUSSI ET AL.

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Interview (Jun 7, 2005).
2. ☒ The allowed claim(s) is/are 14-42 (now renumbered as 1-29, respectively for printing purposes).
3. ☒ The drawings filed on 22 February 2005 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413),  
Paper No./Mail Date 06072005.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

  
TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER

### **SUPPLEMENTAL EXAMINER'S AMENDMENT**

A supplemental examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this supplemental examiner's amendment was given in a telephone interview with the applicants' representative Craig Thompson (Reg. No. 47,990) on Jun 7, 2005.

The application has been amended as follows:

Claim 42, lines 5-6: replaced the phrase "the second differential input being received prior to the first differential input" with --the first differential input being sampled and held to generate the second differential input--.

After being made aware that the first/second differential inputs (with their respective present/previous voltage signals) could be associated with delayed signals, the above change was made to more clearly distinguish the two sets of differential inputs signals over signals that are simply delayed. Other related comments are described later under the Prior Art section.

### ***REASONS FOR ALLOWANCE***

Most of the following reasons for allowance were described in the previous Examiner's Amendment. The main change is related to claim 42, accounting for the amended change.

None of the prior art references reviewed and considered shows/discloses the filtering method, communication system (with a filter circuit), and/or filter circuit as recited within independent claims 14, 25, 29, 33, 38, 40, and 42. More specifically, none of the references

Art Unit: 2816

clearly shows/discloses at least first/second differential pairs (biased by their respective first/second signals, wherein first/second output nodes correspond to transistors receiving their associated signal with the understanding that the signals comprise present and previous type signals (e.g. one signal is received prior to another signal)); and the first/second output terminals (or nodes), wherein the filtering method (or filter circuit) also includes: 1) the first/second differential inputs being weighted as recited within claim 14, upon which claims 15-24 depend; 2) the transistor pairs are biased by the first/second differential inputs received from the same-and-hold circuit as recited within claim 25, upon which claims 26-28 depend; 3) the tail current differential relates to a difference in channel widths as recited within claim 29, upon which claims 30-33 depend; 4) the first/second offset-inducing differential pairs as recited within claim 33, upon which claims 34-37 depend; 5) the differential pair transistors are p-channel MOSFETs as recited within claim 38, upon which claim 39 depends; and 6) the third differential transistor pair is biased by subsequent first/second voltage signals as recited within claim 40, upon which claim 41 depends. Also, none of the references clearly shows or discloses that the first differential input (i.e. present first/second voltage signals) is sampled and help to generate the second differential input (i.e. previous first/second voltage signals) as now recited within claim 42. Since there is no strong motivation to modify or combine any prior art reference(s) to ensure present/previous type signals are applied to their corresponding differential pair, along with the other recited limitation(s) described above with respect to claims 14, 25, 29, 33, 38, 40, and 42, all the active claims (i.e. 14-42) are deemed patentably distinct over the prior art of record.

Claims 14-42 are allowed, and have been renumbered as 1-29, respectively for printing purposes. The renumbering takes into account the cancellation of claims 1-13.

***PRIOR ART***

The prior art reference cited on the accompanying PTO-892 was recently brought to the examiner's attention with respect to what can be considered signals that are received prior to other signals. For example, Fig. 1 of Traa shows first/second differential transistor pairs A0/A1 each receiving their own respective input signals; tail current (i.e. GI0/GI1); and first/second output nodes 16/18. First transistor pair A0 receives signal INPUT, which is also supplied to the input of delay buffer FDB1; and second transistor pair A1 receives the signals output by delay buffer FDB1, and which are also supplied to the input of delay buffer FDB1. These sets of signals can be interpreted in two ways with respect to one set of signals being received prior to the other set of signals. For example, since the output signals of delay buffer FDB1 correspond to its input signals INPUT, any change related to the input signals is received prior to any corresponding change at the output signals. Thus one of ordinary skill in the art can consider the input signals as the second differential input that is received prior to the corresponding output signals (the first differential input). However, what can be considered the first/second differential inputs are reversed in the other interpretation of the signals. When a change is received at the input, the output signals of delay buffer FDB1 do not change for "FD seconds" (i.e. see column 2, lines 55-56), wherein this delay is understood to correspond to the time required for the newly received input signal changes to propagate through the delay buffer completely. Therefore, during this delay period, the output of delay buffer FDB1 still represents the previous (e.g. prior) levels of the input signal, which was received before the new input signals, which now can represent the present input.

With these new interpretations of which signal is received prior to another signal, the other references previously cited (by either the applicants or the examiner) were reviewed and considered. The reference of Crosby appears to be the most relevant, wherein its Fig. 1 clearly shows a DELAY MEANS 50 receiving input signals SAMP1/SAMP2, with its output signals being understood as being delayed versions of the input signals. Therefore, for the same reasoning as described above with respect to the delay buffer FDB1 of Traa, the signals related to Crosby's DELAY MEANS 50 could also be considered as having one set received prior to the other set.

These interpretations of the signals were discussed with the applicants' representative Craig Thompson on Jun 6, and again on Jun 7. After discussing various changes to the broadest claim (i.e. 42), it has now had the phrase "the second differential input being received prior to the first differential input" replaced with --the first differential input being sampled and held to generate the second differential input--. With this change, the new limitations read over the references of Traa and Crosby. There delay related signals are not considered the same as signals that are sampled and held. Also, one of ordinary skill in the art would understand the relationships between the sampled and held differential inputs, with respect to the present/previous voltage signals those differential inputs comprise.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

Art Unit: 2816

The new central official fax number is (703) 872-9306.


Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Terry L. Englund

7 June 2005



TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800